What is claimed is:

1. A method for synchronizing circuitry using a single line, comprising:

charging a first synchronization node that is located on a first die;

comparing a voltage of the first synchronization node with a first reference voltage;

comparing a voltage of the first synchronization node with a second reference voltage that is lower than the first reference voltage;

discharging the synchronization node for a period of time such that the voltage of the first synchronization node falls below the first and second threshold voltages in response to a comparison wherein the voltage of the first synchronization node exceeds the first reference voltage; and

driving circuitry of the first die in response to comparing a voltage of the first synchronization node with a second reference voltage.

2. The method of claim 1, further comprising coupling a capacitor that is not situated on the first die to the first synchronization node.

3. The method of claim 1, further comprising applying an external clock signal that is not generated on the first die to the first synchronization node.

4. The method of claim 1, wherein the driven circuitry on the first die is a PWM switching circuit.

5. The method of claim 1, further comprising:

coupling a second synchronization node that is on a second die that is different from the first die to the first synchronization node such that the voltage of the first synchronization node is substantially equal to the voltage of the second synchronization node;

comparing a voltage of the second synchronization node with a third reference voltage;

comparing a voltage of the second synchronization node with a fourth reference voltage that is lower than the third reference voltage;

discharging the synchronization node for a period of time such that the voltage of the second synchronization node falls below the second, third and fourth threshold voltages in response to a comparison wherein the voltage of the second synchronization node exceeds the third reference voltage; and

driving circuitry of the second die in response to comparing a voltage of the second synchronization node with a fourth reference voltage.

6. The method of claim 5, further comprising coupling a capacitor that is not situated on one of the first and second dice to the first synchronization node.

7. The method of claim 1, further comprising using a constant current source to charge the first synchronization node.

8. A circuit for synchronizing circuitry using a single line, comprising:

means for charging a first synchronization node that is located on a first die;

a first reference voltage comparison means for comparing a voltage of the first synchronization node with a first reference voltage;

a second reference voltage comparison means for comparing a voltage of the first synchronization node with a second reference voltage that is lower than the first reference voltage;

means for discharging the synchronization node for a period of time such that the voltage of the first synchronization node falls below the first and second threshold voltages in response to the first reference voltage comparison means detecting when the voltage of the first synchronization node exceeds the first reference voltage; and

means for driving circuitry of the first die in response to comparing a voltage of the first synchronization node with a second reference voltage.

9. The circuit of claim 8, further comprising means for coupling a capacitor that is not situated on the first die to the first synchronization node.

10. The circuit of claim 8, further comprising means for applying an external clock signal that is not generated on the first die to the first synchronization node.

11. The circuit of claim 8, wherein the driven circuitry on the first die is a PWM switching circuit.

12. The circuit of claim 9, further comprising:

means for coupling a second synchronization node that is on a second die that is different from the first die to the first synchronization node such that the voltage of the first synchronization node is substantially equal to the voltage of the second synchronization node;

a third reference voltage comparison means for comparing a voltage of the second synchronization node with a third reference voltage;

a fourth reference voltage comparison means for comparing a voltage of the second synchronization node with a fourth reference voltage that is lower than the third reference voltage;

means for discharging the synchronization node for a period of time such that the voltage of the second synchronization node falls below the second, third and fourth threshold voltages in response to the third reference voltage comparison means detecting when the voltage of the second synchronization node exceeds the third reference voltage; and

means for driving circuitry of the second die in response to comparing a voltage of the second synchronization node with a fourth reference voltage.

13. The circuit of claim 12, further comprising means for coupling a capacitor that is not situated on one of the first and second dice to the first synchronization node.

14. The circuit of claim 1, further comprising using a constant current source means to charge the first synchronization node.

15. A circuit for synchronizing circuitry using a single line, comprising:

a first current source that is configured to charge a first synchronization node that is located on a first die;

a first comparator that is configured to compare a voltage of the first synchronization node with a first reference voltage;

a second comparator that is configured to compare a voltage of the first synchronization node with a second reference voltage that is lower than the first reference voltage;

a first switching circuit that is configured to discharge the synchronization node for a period of time such that the voltage of the first synchronization node falls below the first and second threshold voltages in response to a comparison wherein the voltage of the first synchronization node exceeds the first reference voltage; and

a first driving circuit that is configured to drive circuitry of the first die in response to the output of the second comparator.

16. The circuit of claim 15, further comprising a capacitor that is not situated on the first die and that is coupled to the first synchronization node.

17. The circuit of claim 15, further comprising an external clock generator that is not on the first die for generating a clock signal that is applied to the first synchronization node.

18. The circuit of claim 15, wherein the driven circuitry on the first die is a PWM switching circuit.

19. The circuit of claim 15, further comprising:

a second current source that is coupled to a second synchronization node that is on a second die that is different from the first die to the first synchronization node and is coupled to the first synchronization node such that the voltage of the first

synchronization node is substantially equal to the voltage of the second synchronization node;

a third comparator that is configured to compare the voltage of the second synchronization node with a third reference voltage;

a fourth comparator that is configured to compare the voltage of the second synchronization node with a fourth reference voltage that is lower than the third reference voltage;

a second switching circuit discharging the synchronization node for a period of time such that the voltage of the second synchronization node falls below the second, third and fourth threshold voltages in response to the third reference voltage comparison means detecting when the voltage of the second synchronization node exceeds the third reference voltage; and

a second driving circuit that is configured to drive circuitry in response to comparing a voltage of the second synchronization node with a fourth reference voltage.

20. The circuit of claim 19, further comprising a capacitor that is not situated on one of the first and second dice and that is coupled to the first synchronization node.